Realization of Device Decomposition for Technology Synthesis with the Genetic Algorithm

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Abstract – To accomplish device decomposition for technology synthesis, it is important to apply some efficient algorithms searching for "acceptability region" of device designables, which satisfy the designed device performance. In this paper, Genetic Algorithm is applied and a prototype system is suggested to solve this problem. The results of the experiment on FIBMOS show that Genetic Algorithm and the proposed system are efficient to deal with device decomposition and study device characteristics. Some potential problems to succeed device decomposition are also discussed in this paper.

1. INTRODUCTION

A new process design methodology called technology synthesis has been explored recently[1][2].

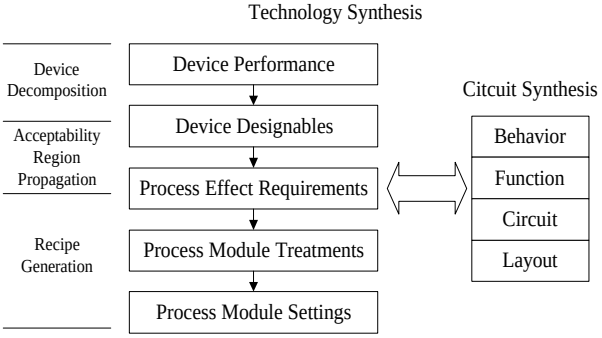

Fig.1 Abstraction levels for technology synthesis and correspondence to circuit synthesis

Technology synthesis employs a top-down approach to process design, starting with the desired results (such as performance, reliability, cost/yield, etc.) and propagating this requirement downward through the process steps. Analogous to the abstraction levels used in circuit design, technology synthesis can also be classified into several abstraction levels [Fig.1], which separate the design problem into several sub-problems that can be potentially solved concurrently.

The top-down synthesis methodology begins with a specification at the highest level of abstraction, device performance. The second highest abstract level is the specification on device designables. So the first step in technology synthesis is to determine the specification on the device designables from the constraints on the device performance. Device performance defines the electrical behavior of the device. Examples are on and off currents, threshold voltage, output resistance, etc. for MOS devices. Device designables are the parameters that specify the topography and impurity concentrations associated with a device. Typical designables are physical gate length, oxide thickness, doping profile descriptors (such as r_p and Δr_p in the Gaussian description of an implanted doping profile), etc. The mapping of performance specifications to a set of acceptable designables is called device decomposition [Fig.2].

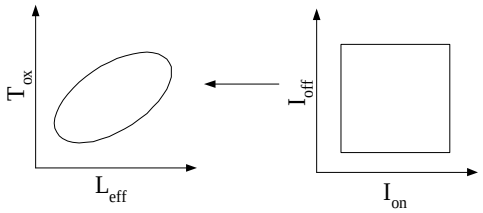

Fig.2 An example of device decomposition

In practice, device decomposition is made difficult by the fact that there are no explicit transformations from the performances to the designables. "Forward" models exist from the designables to the performance. These models are typically encapsulated implicitly in device simulators or compact ones created through experimental data. Because these forward models are usually highly nonlinear, a mathematical inversion of the equations is not possible. Thus, device de-composition is performed through searching over the space of designables specified by the designer. With the forward models and some efficient search algorithms, the space of acceptable device designables

that meet the performance specifications is determined. Instead of considering a single point solution to the device design, the region of acceptable devices in the designable space is considered. This is termed the "acceptability region". The acceptability region is an n-dimensional body when there are n designables of interest.

In this paper, we consider device decomposition as a problem of acquiring acceptability region. Thus, a prototype system is designed to accomplish that aim. The core synthesis algorithm we employed is the Genetic Algorithm[3] (GA) due to its efficient search and optimization ability. Other optimization algorithms, such as constrained variable metric (CVM) algorithm and modified damped least square (MDLS) algorithm[4], are used to help speed up the convergence of GA. As an example, we have applied the proposed system to synthesis the Focused-Ion-Beam (FIB) MOSFET[5][6]. The results show that the aim of device decomposition can be reached with the proposed system.

2. PROTOTYPE SYSTEM

The architecture of the proposed prototype system is summarized in Fig.3. There are four key components within this system (marked with the dashed line).

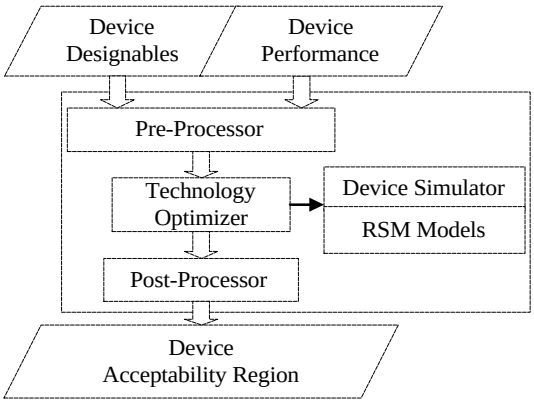

Fig.3 System architecture

Pre-processor

To solve device decomposition efficiently, we suggest a pre-processor should be incorporated to the whole system. There are three main aims: 1) It can accomplish dimension reduction of the device designable space by partitioning the original complex problem into a set of simplified sub-problems. 2) It can accomplish the decoupling of each partitioned sub-problem to a set of synthesis sub-tasks, which are in charge of searching bounds of acceptability region. Through synthesizing bounds of acceptability region, detailed device characteristics can be studied. 3) It can process some checks for device decomposition, including sensitivity analysis of device designables to remove redundant ones, validity check of device performance, etc.

Technology optimizer

To acquire acceptability region, it is necessary to use an efficient random search algorithm, which can produce enough useful solution points to construct bounds of acceptability region while not processing too many redundant computations. GA[3] can exactly provide us this opportunity. GA is a kind of random algorithm that searches the solution space in the direction of optimizing the defined objectives. Further more, it is internal parallel computing, which means GA can explore many schemes through only one genetic operation and computation. During its search process, more computations are run to reach the objective optimization, which ensures that more solution points will be explored to construct bounds of acceptability region.

Gradient-based optimization algorithms[4] are also necessary because of their rapid convergence characteristic near optimal points. By combining GA with MDLS and CVM, bounds of acceptability region can be acquired accurately in a shorter time than by only GA. This is very important because device simulators are usually time-consuming.

Device simulator / RSM models

In our present system, a numerical device simulator PISCES-2ET is used. To speed up device decomposition, analytical or simplified device models should be considered instead of numerical device simulators. Response surface method (RSM) is a potential candidate to deal with the simplification of complex device models. RSM research is under development now.

Post-processor

After the results of device decomposition have been acquired, data analyses should be processed for some

useful device information. Post-processor is used to fit the bounds of acceptability region with some defined functions, such as linear or exponential functions. Thus, some characteristics of acceptability region can be extracted.

3. APPLICATION ON FIBMOS

To demonstrate the conception of device de-composition and the feasibility of the proposed prototype system, we have fulfilled device de-composition on a new-fashion MOSFET: Focused-Ion-Beam (FIB) MOSFET [5][6] [Fig.4].

The device performance of FIBMOS includes on current (I_{on}), off current (I_{off}), and dynamic output resistance (R_{out}). The device designables include lateral implantation position (x), implantation dose, and implantation energy. Here the energy is a doping profile descriptor corresponding with the vertical distance (r_p) and vertical deviation (Δr_p) of the implantation profile at the implanted point. The device performance and device designables are shown in Table 1 and Table 2.

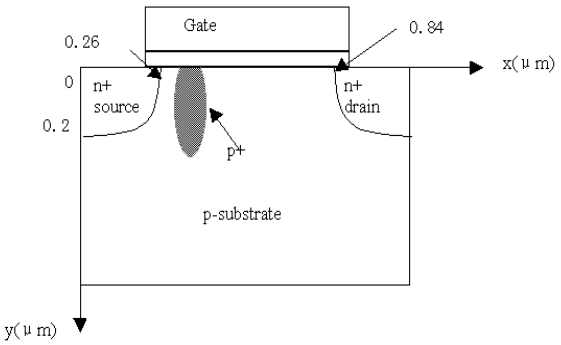

Fig.4 Device structure of FIB MOSFET

Table 1 Device performance of FIBMOS

Name	Objective	Unit
I_{on}	1.2e-4≤I_{on}≤1.5e-4	A/μm
I_{off}	I_{off}≤1e-12	A/μm
R_{out}	R_{out}≥8e4	Ω

Table 2 Device designables of FIBMOS

Name	Min	Max	Unit
X	0.25	0.55	μm
Dose	2e13	2e16	cm^{-2}
Energy	10	200	Kev

The solving problem is partitioned into three sub-problems : (*a*) search for acceptability region of (dose, energy) when x is fixed at some specific values; (*b*) search for acceptability region of (dose, x) when energy is fixed at some specific values; (*c*) search for acceptability region of (energy, x) when dose is fixed at some specific values. Then each sub-problem is divided into four sub-tasks:

Task①: I_{on}=1.2e-4, satisfying I_{off}≤1e-12, R_{out}≥8e4

Task②: I_{on}=1.5e-4, satisfying I_{off}≤1e-12, R_{out}≥8e4

Task③: I_{off}=1e-12, satisfying 1.2e-4≤I_{on}≤1.5e-4, R_{out}≥8e4

Task④: R_{out}=8e4, satisfying 1.2e-4≤I_{on}≤1.5e-4, I_{off}≤1e-12

Each sub-task may acquire one bound of acceptability region. Finally, to ensure that I_{on} can fall in the range of 1.2e-4A/μm and 1.5e-4A/μm under the given I_{off} and R_{out} constraints, CVM is performed to maximize the I_{on} when satisfying the constraints. The result is that I_{on} can reach over 1.5e-4A/μm with the designed FIB device structure. So the design of FIBMOS decomposition is appropriate.

To evaluate all kinds of objectives, different evaluation functions for GA are designed as the following:

Equal objective (For example, I_{on}=1.2e-4)

EE = (I_{on}-1.2e-4)/1.2e-4, when I_{on}≥1.2e-4

(1.2e-4-I_{on})/I_{on}, when I_{on}<1.2e-4

Lower objective (For example, R_{out}≥8e4)

EL = weight*(8e4-R_{out})/ R_{out}, when R_{out}<8e4

0, when R_{out}≥8e4

Upper objective (For example, I_{off}≤1e-12)

EU = weight*(I_{off} -1e-12)/1e-12, when I_{off}>1e-12

0, when I_{off}≤1e-12

Total evaluation result (Acceptable error)

ER = EE + EL + EU

For each sub-task with GA, about 550 device simulations are run, which cost about two and a half hours with the Ultra60 workstation. The acceptable error for GA is 1%, which means that all solution points with the evaluation result below 1% are extracted to construct bounds of acceptability region.

For sub-task① of sub-problem (*c*) the results are shown as Fig.5. The relationship of (energy, x), fitted with linear and exponential functions in different regions can be interpreted through the relationship of V_{th} and x [Fig.6] by three-transistor model of FIBMOS[6]. To compensate the reduction of V_{th} when

the lateral FIB position moves close to the source, the energy of FIB should diminish as Fig.5 if the dose of FIB is fixed.

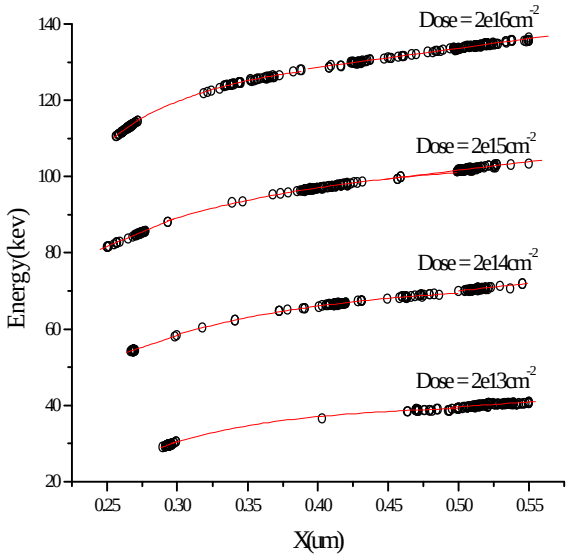

Fig.5 Synthesis results of sub-task① of sub-problem (*c*)

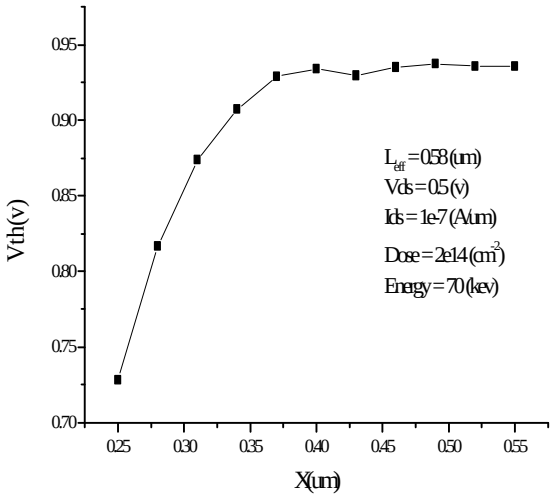

Fig.6 Relationship of Vth vs. X (the lateral FIB position) when the dose and the energy of FIB are fixed

For all sub-tasks of sub-problem (*c*) the result at a specific dose value (2e14cm^{-2}) is shown as Fig.7. The region encompassed by three synthesized bounds and the lower and upper bounds of x (the dashed region) is just what we really want - acceptability region of (energy, x) at the specific dose value. The reason that the bound of sub-task④ isn't shown is that all solution points will certainly satisfy the R_{out} objective once they have satisfied the I_{on} and I_{off} objectives. Data from all sub-tasks of all sub-problems can help us to construct a 3-dimension acceptability region of (energy, dose, x). This 3-dimension acceptability region has three bound planes corresponding with sub-task①, ②, and ③, respectively. Further tests on points in the acquired acceptability region show that they all satisfy the deigned device performance.

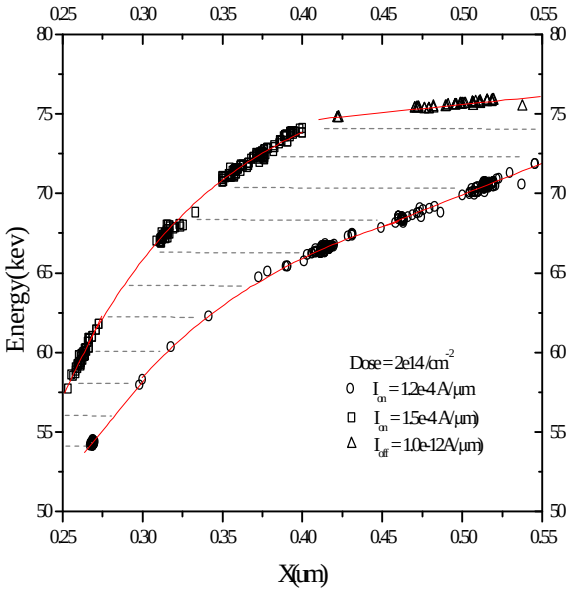

Fig.7 Synthesis results of all sub-tasks of sub-problem (*c*) at a specific dose value (2e14cm^{-2})

The channel length effect on FIBMOS is also studied with this prototype system, the synthesis results of sub-task① of sub-problem (*c*) at a specific dose value (2e15cm^{-2}) for different channel lengths are shown as Fig.8. When the channel length is reduced, the on current will increase if all others are fixed. So to achieve the same on current, the implantation energy must also be reduced if the implantation position and the implantation dose of FIB are fixed. It is an interesting result that the channel length effect is very weak [Fig.8] when the FIB implantation position is close to the source. So MOSFET with a next-to-source FIB implantation will achieve a stabilized threshold voltage when the channel length is reduced[5], which indicates a potential application of FIBMOS in the sub-micron

device fields.

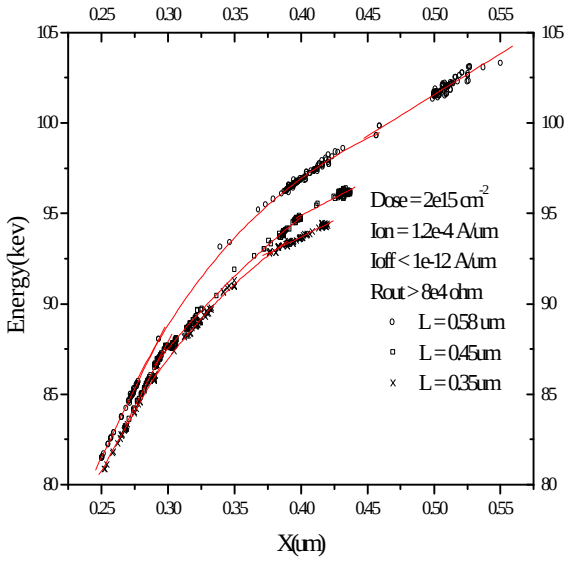

Fig.8 Synthesis results of sub-task① of sub-problem (*c*) at the dose value (2e15cm^{-2}) for different channel lengths

4. CONCLUSIONS

A prototype system is suggested to solve device de-composition for technology synthesis, with GA as its core synthesis algorithm. The experiment on FIBMOS shows the aim of device decomposition is reached with the system. Based on the acceptability region, engineers can perform the next step of technology synthesis. Further more, by analyzing the acquired acceptability region, some unknown or ignored device characteristics can be explored. So this system is also useful for researchers to study new devices.

5. ACKNOWLEDGEMENT

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